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PLUS Search Results for S/N 09866005, Searched September 02, 2004

The Patent Linguistics Utility System (PLUS) is a USPTO automated search system for U.S. Patents from 1971 to the present. PLUS is a query-by-example search system which produces a list of patents that are most closely related linguistically to the application searched. This search was prepared by the staff of the Scientific and Technical Information Center, SIRA.

5790831

5867645

5974495

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09866005_LIST

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09866005_QUAL

5790831 99
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5974495 99
5978860 99
5721497 97
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5247642 92
5274783 92

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5313594 92

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09866005_CLS
Most Frequently Occurring Classifications of Patents Returned
From A Search of 09866005 on September 02, 2004

Original Classifications

8 710/305
4 365/233
4 710/104
3 710/315
3 711/105
2 365/194
2 710/105
2 713/400

Cross-Reference Classifications

6 365/230.02
5 365/189.02
5 365/233
4 710/3
4 710/51
4 710/61
4 710/9
3 710/36
2 365/194
2 365/230.03
2 710/315
2 711/170
2 713/400
2 713/401
2 713/500

Combined Classifications

9 365/233
8 710/305
6 365/230.02
5 365/189.02
5 710/315
4 365/194
4 710/104
4 710/3
4 710/36
4 710/51
4 710/61
4 710/9
4 711/105
4 713/400
3 365/230.03
3 710/105

09866005_CLS

2 710/113
2 710/260
2 711/170
2 713/401
2 713/500

09866005_CLSTITLES

Titles of Most Frequently Occurring Classifications of Patents Returned

From A Search of 09866005 on September 02, 2004

9 365/233 (4 OR, 5 XR)
 Class 365 : STATIC INFORMATION STORAGE AND RETRIEVAL
 365/230.01 ADDRESSING
 365/233 .Sync/clocking

8 710/305 (8 OR, 0 XR)
 Class 710 : ELECTRICAL COMPUTERS AND DIGITAL DATA
 PROCESSING SYSTEMS: INPUT/OUTPUT
 710/100 INTRASYSTEM CONNECTION (E.G., BUS AND BUS
 TRANSACTION PROCESSING)
 710/305 .Bus interface architecture

6 365/230.02 (0 OR, 6 XR)
 Class 365 : STATIC INFORMATION STORAGE AND RETRIEVAL
 365/230.01 ADDRESSING
 365/230.02 .Multiplexing

5 365/189.02 (0 OR, 5 XR)
 Class 365 : STATIC INFORMATION STORAGE AND RETRIEVAL
 365/189.01 READ/WRITE CIRCUIT
 365/189.02 .Multiplexing

5 710/315 (3 OR, 2 XR)
 Class 710 : ELECTRICAL COMPUTERS AND DIGITAL DATA
 PROCESSING SYSTEMS: INPUT/OUTPUT
 710/100 INTRASYSTEM CONNECTION (E.G., BUS AND BUS
 TRANSACTION PROCESSING)
 710/305 .Bus interface architecture
 710/306 ..Bus bridge
 710/315 ...Different protocol (e.g., PCI to ISA)

4 365/194 (2 OR, 2 XR)
 Class 365 : STATIC INFORMATION STORAGE AND RETRIEVAL
 365/189.01 READ/WRITE CIRCUIT
 365/191 .Signals
 365/194 ..Delay

4 710/104 (4 OR, 0 XR)
 Class 710 : ELECTRICAL COMPUTERS AND DIGITAL DATA
 PROCESSING SYSTEMS: INPUT/OUTPUT
 710/100 INTRASYSTEM CONNECTION (E.G., BUS AND BUS
 TRANSACTION PROCESSING)
 710/104 .System configuring

09866005_CLSTITLES

4	710/3	(0 OR, 4 XR)
	Class	710 : ELECTRICAL COMPUTERS AND DIGITAL DATA PROCESSING SYSTEMS: INPUT/OUTPUT
	710/1	INPUT/OUTPUT DATA PROCESSING
	710/3	.Input/Output addressing
4	710/36	(1 OR, 3 XR)
	Class	710 : ELECTRICAL COMPUTERS AND DIGITAL DATA PROCESSING SYSTEMS: INPUT/OUTPUT
	710/1	INPUT/OUTPUT DATA PROCESSING
	710/36	.Input/Output access regulation
4	710/51	(0 OR, 4 XR)
	Class	710 : ELECTRICAL COMPUTERS AND DIGITAL DATA PROCESSING SYSTEMS: INPUT/OUTPUT
	710/1	INPUT/OUTPUT DATA PROCESSING
	710/36	.Input/Output access regulation
	710/51	..Accessing via a multiplexer
4	710/61	(0 OR, 4 XR)
	Class	710 : ELECTRICAL COMPUTERS AND DIGITAL DATA PROCESSING SYSTEMS: INPUT/OUTPUT
	710/1	INPUT/OUTPUT DATA PROCESSING
	710/58	.Input/Output process timing
	710/61	..Synchronous data transfer
4	710/9	(0 OR, 4 XR)
	Class	710 : ELECTRICAL COMPUTERS AND DIGITAL DATA PROCESSING SYSTEMS: INPUT/OUTPUT
	710/1	INPUT/OUTPUT DATA PROCESSING
	710/8	.Peripheral configuration
	710/9	..Address assignment
4	711/105	(3 OR, 1 XR)
	Class	711 : ELECTRICAL COMPUTERS AND DIGITAL PROCESSING SYSTEMS: MEMORY
	711/100	STORAGE ACCESSING AND CONTROL
	711/101	.Specific memory composition
	711/104	..Solid-state random access memory (RAM)
	711/105	...Dynamic random access memory
4	713/400	(2 OR, 2 XR)
	Class	713 : ELECTRICAL COMPUTERS AND DIGITAL PROCESSING SYSTEMS: SUPPORT
	713/400	SYNCHRONIZATION OF CLOCK OR TIMING SIGNALS, DATA, OR PULSES

09866005_CLSTITLES

- 3 365/230.03 (1 OR, 2 XR)
 Class 365 : STATIC INFORMATION STORAGE AND RETRIEVAL
 365/230.01 ADDRESSING
 365/230.03 .Plural blocks or banks
- 3 710/105 (2 OR, 1 XR)
 Class 710 : ELECTRICAL COMPUTERS AND DIGITAL DATA
 PROCESSING SYSTEMS: INPUT/OUTPUT
 710/100 INTRASYSTEM CONNECTION (E.G., BUS AND BUS
 TRANSACTION PROCESSING)
 710/105 .Protocol
- 2 710/113 (1 OR, 1 XR)
 Class 710 : ELECTRICAL COMPUTERS AND DIGITAL DATA
 PROCESSING SYSTEMS: INPUT/OUTPUT
 710/100 INTRASYSTEM CONNECTION (E.G., BUS AND BUS
 TRANSACTION PROCESSING)
 710/107 .Bus access regulation
 710/113 ..Centralized bus arbitration
- 2 710/260 (1 OR, 1 XR)
 Class 710 : ELECTRICAL COMPUTERS AND DIGITAL DATA
 PROCESSING SYSTEMS: INPUT/OUTPUT
 710/260 INTERRUPT PROCESSING
- 2 711/170 (0 OR, 2 XR)
 Class 711 : ELECTRICAL COMPUTERS AND DIGITAL PROCESSING
 SYSTEMS: MEMORY
 711/100 STORAGE ACCESSING AND CONTROL
 711/170 .Memory configuring
- 2 713/401 (0 OR, 2 XR)
 Class 713 : ELECTRICAL COMPUTERS AND DIGITAL PROCESSING
 SYSTEMS: SUPPORT
 713/400 SYNCHRONIZATION OF CLOCK OR TIMING SIGNALS,
 DATA, OR PULSES
 713/401 .Using delay
-
- 2 713/500 (0 OR, 2 XR)
 Class 713 : ELECTRICAL COMPUTERS AND DIGITAL PROCESSING
 SYSTEMS: SUPPORT
 713/500 CLOCK, PULSE, OR TIMING SIGNAL GENERATION OR
 ANALYSIS